AF

WILLIAMS, MORGAN & AMERSON, P.C.

10333 RICHMOND, STE. 1100, HOUSTON, TEXAS 77042

(713) 934-7000 FAX: (713) 934-7011

Danny L. Williams
Terry D. Morgan
J. Mike Amerson
Kenneth D. Goodman
Jeffrey A. Pyle
Jaison C. John
Ruben S. Bains
Paul R. Juhasz

Raymund F. Eich, Ph.D.*
Mark W. Sincell, Ph.D.*
Sanjeev K. Singh, Ph.D.*

*Patent Agent

Writer's Direct Dial
713.934.4069

FILE: 2000.075200

June 6, 2005

CERTIFICATE OF MAILING
37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 6, 2005 by:

SIGNATURE

CUSTOMER NO. 23720

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RE: *U.S. Patent Application Serial No. 09/909,074*
Entitled: "METHOD AND APPARATUS FOR CONTROLLING A THICKNESS OF A CONDUCTIVE LAYER IN A SEMICONDUCTOR MANUFACTURING OPERATION"
Inventor(s): JOYCE S. OEY HEWETT and ALEXANDER J. PASADYN
Client's Reference: TT4629

Sir:

Transmitted herewith for filing are:

1. An Appeal Brief;

2. A return postcard to acknowledge receipt of these materials. Please date stamp and mail this postcard.

The Director is authorized to deduct the fee ($500) for filing this Appeal Brief and any other fees required under 37 C.F.R. §§ 1.16 to 1.21 from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT4629[1].

Please date stamp and return the enclosed postcard to evidence receipt of these materials.

[1] In the event the monies in that account are insufficient, the Director is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50 0786/2000.075200.

Respectfully submitted,
WILLIAMS, MORGAN & AMERSON

Date: June 6th, 2005

Jaison C. John
Reg. No. 50,737
Attorney for Applicants

WILLIAMS, MORGAN & AMERSON
CUSTOMER NUMBER: 23720
10333 Richmond Dr., Suite 1100
Houston, Texas 77042
(713) 934-4069 ph
(713) 934-7011 fx

CERTIFICATE OF MAILING 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: MS Appeal Brief – Patents; Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this the 6th day of June, 2005.

Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JOYCE S. OEY HEWETT ALEXANDER J. PASADYN	Group Art Unit:	2823
		Examiner:	KHIEM D. NGUYEN
Serial No.:	09/909,074	Conf. No.:	9763
Filed:	JULY 19, 2001	Atty. Dkt.:	2000.075200/TT4629
For:	METHOD AND APPARATUS FOR CONTROLLING A THICKNESS OF A CONDUCTIVE LAYER IN A SEMICONDUCTOR MANUFACTURING OPERATION	CUSTOMER NO.:	23720

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On April 4, 2005, Appellants filed a Notice of Appeal in response to a Final Office Action dated January 1, 2005, issued in connection with the above-identified application. In support of the appeal, Appellants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences.

Since the Notice of Appeal for the present invention was received and stamped by the USPTO Mailroom on April 6, 2005, the two-month date for filing this Appeal Brief is June 6, 2005. Since this Appeal Brief is being filed on June 6, 2005, this paper is believed to be timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500.00) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT4629. No other fee is believed to be due in connection with the filing of this document. However, should any fee under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this document, the Commissioner is hereby authorized to deduct said fee from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.075200.

Please date stamp and return the enclosed postcard to evidence receipt of this document.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1, 2, 4-13, and 15 are pending in this application. Claims 3 and 14 have been canceled and claims 16-41 have been withdrawn from consideration. Accordingly, claims 1, 2, 4-13, and 15 are the subject of the present appeal.

Claim 1, 2, 4-13, and 15 were rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent Application Publication No. 2002/0032499 to ***Wilson et al. (Wilson)*** in view of the U.S. Patent No. 6,685,814 to ***Uzoh et al (Uzoh).***

The claims currently under consideration, *i.e.*, claims 1, 2, 4-13, and 15, are listed in the Claims Appendix.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the present invention is directed to several inventive methods and apparatus for controlling a thickness of a deposited layer in a semiconductor manufacturing operation.

Embodiments of the present invention provide for a method of controlling a conductive layer deposition process that includes depositing a conductive layer onto a semiconductor wafer based upon a deposition recipe, measuring a thickness of the conductive layer deposited on the semiconductor wafer, determining whether the measured thickness of the conductive layer is within a predetermined tolerance, and revising the deposition recipe if the thickness of the conductive layer is not within the predetermined tolerance. Embodiments of the present

invention call for an apparatus that includes a deposition unit capable of depositing a conductive layer according to a deposition recipe; a thickness measuring unit capable of measuring at least one thickness of the conductive layer and outputting thickness data; and a deposition control unit capable of receiving the thickness data from the thickness measuring unit, determining whether the thickness data is within a predetermined tolerance, revising the deposition recipe if the thickness data is not within the predetermined tolerance, and outputting the revised deposition recipe.

A transistor 100 in an intermediate state during its manufacture is shown in Figure 1. The transistor 100 is generally comprised of a trench isolation structure 102, a gate insulating layer 104, a gate electrode 106, a sidewall spacer 108, and a plurality of source/drain regions 110. The trench isolation structure 102 may be formed by forming a stop layer made of, for example, silicon nitride on the semiconducting substrate 114, patterning the stop layer, and etching the stop layer and the semiconducting substrate through the opening patterned in the layer of insulating material to form a trench 112. The trench may then be filled with an insulating material (*e.g.*, silicon dioxide, silicon oxynitride, or the like), polishing away excess insulating material using the stop layer (*e.g.*, silicon nitride) as a stop, and wet etching to remove the stop layer. *See* Specification, pg. 6, line 22 – pg. 7, line 11.

The gate insulation layer 104 may then be formed on the semiconducting substrate 114 by a variety of known techniques, *e.g.*, a thermal oxidation process or a deposition process, and may be formed from a variety of materials, such as silicon dioxide. Thereafter, the gate electrode 106 may be formed above the gate insulating layer 104 by depositing a layer formed from a variety of materials, such as polysilicon, and then etching the layer to define the gate

electrode 106. The sidewall spacers 108 may be then formed by conformally depositing a layer of insulating material (*e.g.*, silicon dioxide, silicon nitride, silicon oxynitride, or the like) over the gate electrode 106 and the upper surface 116 of the semiconducting substrate 114 and then performing an anisotropic etching process to remove all of the conformally-deposited layer except a portion adjacent the sidewalls 118 of the gate electrode 106. The source/drain regions 110 may be formed by one or more ion implantation processes in which a dopant material is implanted into the semiconducting substrate 114. Thereafter, an insulating layer 120, made of, for example, silicon dioxide, silicon nitride, silicon oxynitride, or the like, may be formed over the previously formed structures. One or more openings 122 (*e.g.*, vias or trenches) may be then etched through the insulating layer 120. *See* Specification, pg. 7, line 12 – pg. 8, line 3.

As illustrated in Figure 2, a barrier metal layer 202 (*e.g.*, titanium nitride, tantalum, tantalum nitride, or the like) may be deposited over the insulating layer 120 to inhibit migration of copper (deposited in a later process step) into silicon structures. A copper seed layer 204 may then be deposited over the barrier metal. Thereafter, a copper layer 206 may be deposited, typically by a electrolytic plating process, over the copper seed layer 204 to fill the openings 122 (Figure 1). This process typically produces the copper layer 206 across the entire wafer. Once a sufficiently thick copper layer 206 has been deposited, the copper layer 206 may be planarized using CMP techniques. In the example illustrated in Figures 1 and 2, the copper layer 206 is applied to the wafer to provide contacts 208 to source/drain regions 110. After planarizing the copper layer 206, further insulating layers (similar to the insulating layer 120) may be applied to the wafer, etched to form additional openings (*e.g.*, trenches and the like), and filled with copper to form electrical interconnections between the previously formed contacts and the like. Thus, the process of applying an insulating layer, etching the insulating layer to form openings,

depositing a copper layer thereover, and planarizing the copper layer is repeated as desired to form multilevel metal schemes, such as dual damascene schemes. *See* Specification, pg. 8, lines 5 – 21.

It is generally advantageous to optimize the thickness of a copper layer (*e.g.*, the copper layer 206) so that the copper layer 206 is sufficiently thick to properly conduct electrons as required and is sufficiently thin so that the time and materials required to planarize the copper layer are held to a minimum. Further, it is generally advantageous to optimize the thickness of the copper layer 206 on a wafer-by-wafer basis so that variations in thicknesses of copper layers (*e.g.*, the copper layer 206) on a series of wafers are minimized. Referring now to Figure 3, the illustrated embodiment comprises depositing a conductive layer (*e.g.*, the copper layer 206) on a wafer *J* (block 302), wherein *J* represents a wafer number in a series or lot of wafers. After the conductive layer has been deposited, the thickness of the conductive layer is measured (block 304) and is compared to a predetermined, acceptable thickness tolerance to determine if the thickness of the conductive layer is within acceptable limits (block 306). If the thickness of the conductive layer is not within tolerance, the deposition recipe is revised (block 308) so that the conductive layer on the next wafer (i.e., wafer *J*+1) will have a thickness that is within tolerance. The deposition recipe for an electroplating process controls, for example, the electroplating bath temperature, electroplating chemical concentrations, anode-cathode spacing, the anode power settings, the electroplating deposition time, and the like so that the electroplating process will give the desired thickness of the conductive layer. If, however, the thickness of the conductive layer is within tolerance, the next wafer (i.e., wafer *J*+1) is processed (blocks 310, 302) with no changes to the deposition recipe. *See* Specification, pg. 8, line 24 – pg. 9, line 22.

In the embodiment illustrated in Figures 4 and 5, the thickness of the conductive layer 502 on a semiconductor wafer 504 is measured (block 304) by measuring a thickness at a plurality of points 506 (only one labeled) on the conductive layer 502 (block 402). A value is calculated that represents the thickness measurements in the aggregate (block 404). The calculated thickness value can be any other representation that adequately reflects the measured thicknesses in the aggregate. In one embodiment, the calculated thickness value is an average of the measured thicknesses, *e.g.*, an arithmetic mean, a median, a mode, a geometric mean, a harmonic mean, a quadratic mean, or the like, of the measured thicknesses. In one embodiment, a measure of dispersion of the data about the calculated thickness value is used to determine whether the layer thickness is within tolerance (block 306) by comparing the measure of dispersion to a predetermined statistical distribution. For example, the measure of dispersion can be a mean deviation, a quartile deviation, a standard deviation, or the like, of the measured thicknesses about the average of the measured thicknesses. The predetermined statistical distribution can be, for example, a normal distribution, a binomial distribution, a Poisson distribution, a multinomial distribution, or the like. *See* Specification, pg. 10, lines 1 – 17

While 25 points 506 at which thickness measurements are taken are illustrated in Figure 5, any suitable number of points 506 in a predetermined pattern can be utilized. Further, while a rectilinear array of points 506 is illustrated in Figure 5, any suitable distribution of points 506 can be used. *See* Specification, pg. 10, lines 19 – 22.

Referring now to Figure 6, a workpiece 600 (*e.g.*, a semiconducting substrate or wafer having one or more process layers and/or semiconductor devices disposed thereon) is delivered to a deposition unit 602 that deposits a conductive layer (not shown) on the workpiece 600. The workpiece 600 is then delivered to a thickness measurement unit 604 that measures the thickness of the conductive layer deposited on the workpiece by the deposition unit 602. Thickness data 608 resulting from the thickness measurement unit 604 can be a single thickness measurement or can be a calculated value corresponding to a plurality of thickness measurements, as illustrated in Figures 4 and 5. Using a system communication bus 606, data and/or instructions may be exchanged between any or all of the various units illustrated in Figure 6 or that are otherwise part of the system comprising the units illustrated in Figure 6. Thickness data 608 is sent from the thickness measurement unit 604 to the deposition control unit 610, wherein the thickness data 608 is evaluated to determine if the thickness of the conductive layer on the workpiece 600 is within tolerance. If the thickness is not within tolerance, appropriate changes are made to the deposition recipe by the deposition control unit 610 and the revised deposition recipe is provided as feedback 612 to the deposition unit 602. In the illustrated embodiment, the deposition control unit 610 also provides information corresponding to the feedback 612 (represented by arrow 613) to a supervisory control 614 that may act as an overall manufacturing system supervisory control loop, which may then provide the revised deposition recipe as feedback 616. Rather than providing a revised process recipe, it is within the scope of the present invention for the deposition control unit 610 to calculate bias information and to provide bias information to the supervisory control unit 614 (represented by the arrow 513) and as feedback 612 to the deposition unit 602, and further for the supervisory control unit 614 to provide the bias information as feedback 616 to the deposition unit 602. In this embodiment, the bias information

corresponds to the changes to be made in the deposition unit 602 to correct for unacceptable variation in conductive layer thickness. *See* Specification, pg. 11, line 1 – pg. 12, line 5.

As illustrated in Figure 7, a workpiece 700 (*e.g.*, a semiconducting substrate or wafer having one or more process layers and/or semiconductor devices disposed thereon) is delivered to a deposition tool 702 having a deposition tool controller 704. The deposition tool 702 deposits a conductive layer (not shown) onto the workpiece 700. The workpiece 700 is then delivered to a thickness measurement tool 706 having a measurement tool controller 708. The measurement tool 706 measures the thickness of the conductive layer deposited on the workpiece by the deposition tool 702. Thickness data, which can be a single thickness measurement or can be a calculated value corresponding to a plurality of thickness measurements, as illustrated in Figures 4 and 5, is sent via a line 710 from the measurement tool controller 708 to a computer 712, wherein the thickness data is evaluated to determine if the thickness of the conductive layer on the workpiece 700 is within tolerance. If the thickness is not within tolerance, appropriate changes are made to the deposition recipe by the computer 712 and the revised deposition recipe is provided to the deposition tool controller 704 via line 714. *See* Specification, pg. 12, lines 7 – 21.

Rather than the computer 712 providing a revised process recipe to the deposition tool controller 704, it is within the scope of the present invention for the computer 712 to provide bias information to the deposition tool controller. In this embodiment, the bias information corresponds to the changes to be made in the deposition process to be performed on the next workpiece (not shown) by the deposition tool 702. *See* Specification, pg. 12, line 23 – pg. 13, line 4.

In one embodiment of the present invention, a database 716 stores a plurality of models that might potentially be applied, depending upon the current state of parameters being in use by the deposition tool 702 and the thickness information from the measurement tool 706 and/or the measurement tool controller 708. The computer system 712 then extracts an appropriate model from the database 716 of potential models to apply the identified characteristic parameters. If the database 716 does not comprise an appropriate model, then the characteristic parameter may be ignored or the computer system 712 may attempt to develop one, if so programmed. The database 716 may be stored on any kind of computer-readable program storage medium, for example an optical disk 718, a floppy disk 720, or a hard disk drive (not shown) of the computer system 712. The database 712 may also be stored on a separate computer system (not shown) that interfaces with the computer system 712. *See* Specification, pg. 13, lines 6 – 18.

Modeling of the identified characteristic parameters may be implemented differently in alternative embodiments. For instance, the computer system 712 may be programmed using some form of artificial intelligence to analyze deposition process results (*e.g.*, layer thickness, layer uniformity, etc.) and controller inputs to develop a model on-the-fly in a real-time implementation. In certain situations, this approach can be a useful adjunct to the embodiment illustrated in Figure 7 and discussed above, wherein characteristic parameters are measured and identified for which the database 716 has no appropriate model. *See* Specification, pg. 13, line 20 – pg. 14, line 3.

As is evident from the discussion above, some features of the present invention may be implemented in software. For instance, the acts set forth in the blocks 302-310 in Figure 3 and

blocks 402 and 404 in Figure 4 are, in certain embodiments, software-implemented, in whole or in part. Thus, some features of the present invention are implemented as instructions encoded on a computer-readable program storage medium. The program storage medium may be of any type suitable to the particular implementation. However, the program storage medium will typically be magnetic, such as the floppy disk 720 or the computer 712 hard disk drive (not shown), or optical, such as the optical disk 718. When these instructions are executed by a computer, they perform the disclosed functions. The computer may be a desktop computer, such as the computer 712. However, the computer might alternatively be a processor embedded in the deposition tool 702 or in the measurement tool 706. The computer might also be a laptop, a workstation, or a mainframe in various other embodiments. The scope of the invention is not limited by the type or nature of the program storage medium or computer with which embodiments of the invention might be implemented. *See* Specification, pg. 14, lines 5 – 20.

More specifically, there are two independent claims at issue in the current appeal: claims 1 and 6. Independent claim 1 is generally directed to a method of controlling a conductive layer deposition process. The method of claim 1 involves depositing a conductive layer (502) above a first semiconductor wafer (504) based upon a deposition recipe, measuring a thickness of the conductive layer deposited on the semiconductor wafer (504), determining whether the measured thickness of the conductive layer (502) is within a predetermined tolerance, and revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 9, l. 5 – p. 10, l. 22; Figures 3, 4, and 5. As set forth

in the specification at, for example, page 9, ll. 6 – 18, by measuring thickness of a conductive layer, a chemical concentration parameter of an electroplating bath of a deposition recipe may be selectively revised. Further, the specification sets forth at, for example, page 11, ll. 15 – 21, that a feedback control routine is employed to control a thickness of a conductive layer in a semiconductor manufacturing operation, in response to a chemical adjustment of the deposition recipe.

Independent claim 6 is generally directed to a method of controlling a conductive layer deposition process. The method of claim 6 involves depositing a conductive layer (502) above a first semiconductor wafer (504) based upon a deposition recipe, measuring a thickness of the conductive layer (502) at a plurality of locations, calculating a value representing the measured thickness measured at the plurality of locations, determining whether the calculated value is within a predetermined tolerance, and revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe based upon at least the calculated value if the calculated value is not within the predetermined tolerance. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 9, l. 5 – p. 10, l. 22; Figures 3, 4, and 5.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1, 2, and 6-12 are unpatentable under 35 U.S.C. § 103(a) under U.S. Patent Application Publication No. 2002/0032499 to ***(Wilson)*** in view of the U.S. Patent No. 6,685,814 to ***(Uzoh)***.

2. Whether claims 4 and 15 are unpatentable over ***Wilson*** in view of ***Uzoh***.

3. Whether claims 5 and 13 are unpatentable over ***Wilson*** in view of ***Uzoh***.

VII. ARGUMENT

The present invention is directed to controlling a conductive layer deposition process. *See*, Specification, page 9, line 5. The present invention calls for depositing a conductive layer (502) above a first semiconductor wafer (504) based upon a deposition recipe, measuring a thickness of the conductive layer deposited on the semiconductor wafer (504), determining whether the measured thickness of the conductive layer (502) is within a predetermined tolerance, and revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance. *See*, Specification, page 9, line 5 – page 10, line 22.

The Examiner relies heavily on ***Wilson*** to reject the pending claims in the instant patent application. In contrast to the various embodiments of the claimed invention, ***Wilson*** is directed to an automatic process control for controlling a material deposition process. ***Wilson*** is directed to tuning electrodes 58 for refining electrical parameters when processing a microelectronic workpiece 25. ***Wilson*** calls for making a first determination as to how a baseline set of anode currents should be varied to produce the specified target plating material thicknesses. ***Wilson*** further provides for making a second determination to vary the set of anode currents for a first electroplating cycle to produce the specified target plating material thicknesses. However, ***Wilson*** does not call for the baseline setting of the anode currents to produce the measured

plating material thicknesses of the first workpiece. See the third and sixth method steps of claim 1 on page 10 of ***Wilson***.

The Examiner also relies on ***Uzoh*** to reject the pending claims in the instant patent application. However, ***Uzoh*** does not make for the deficit of ***Wilson***. ***Uzoh*** is directed to enhancing the uniformity of electrodeposition or electroetching to uniformly deposit or etch a thin metal layer or an alloy layer on a semiconductor wafer substrate. See Col. 2 ll. 58-67. ***Uzoh*** does not disclose revising a chemical concentration parameter to produce a desired plating material thickness based on the measured thickness of the plating material layer. ***Uzoh*** does not provide selectively revising a chemical concentration parameter of the electroplating bath of the deposition recipe across the entire conductive layer based on the measured thickness of the conductive layer. Therefore, ***Uzoh*** does not make-up for the deficit of ***Wilson***. The combination of ***Wilson*** and ***Uzoh*** do not teach or make obvious all of the elements of claims of the present invention.

The specific claims of the present invention are discussed below.

A. Claims 1, 2, and 6-12 Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Wilson* in view of *Uzoh*

As the Board well knows, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest

all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

Appellants respectfully assert that the Examiner did not meet the legal standards to reject the claims of the present invention under 35 U.S.C. § 103(a) because the prior art references

(***Wilson*** and ***Uzoh***) do not teach or suggest all the claim limitations of the claims of the present invention. Additionally, the Examiner has not provided sufficient evidence or arguments that there is a suggestion that one skilled in the art would have been motivated to combine the references (***Wilson*** and ***Uzoh***). In fact, Appellants provide arguments that ***Wilson*** and ***Uzoh*** would not have been combined by one skilled in the art. Therefore, the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regarding to claims 1, 2 and 6-12 of the present invention.

Claims 1, 2 and 6-12 stand rejected as unpatentable under 35 U.S.C. § 103(a) by ***Wilson*** in view of ***Uzoh***. Appellants respectfully assert that the Examiner erred in making this rejection.

Group I Claims (Claims 1, 2 and 6-12) Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Wilson* in view of *Uzoh*

Claim 1 of the present invention calls for "revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance," while claim 6 includes the step of "revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe based upon at least the calculated value if the calculated value is not within the predetermined tolerance." These features are not disclosed, taught, or made obvious by ***Wilson***, ***Uzoh***, nor their combination.

It is respectfully submitted that neither ***Wilson*** nor ***Uzoh***, nor any other art of record, disclose the entirety of the steps set forth in independent claims 1 and 6. More specifically, none

of the art of record discloses or makes obvious the subject matter of revising a chemical concentration parameter of a deposition recipe to produce a desired thickness based on the measurement thickness or revising a chemical aspect of the deposition recipe itself across the entire conductive layer based on the measured thickness thereof.

Wilson is directed to an automatic process control for controlling a material deposition process. By tuning electrodes 58, electrical parameters in a processing chamber are refined when processing a microelectronic workpiece 25. For example, ***Wilson*** discloses that a first determination is made as to how a baseline set of anode currents should be varied to produce a specified target plating material thicknesses. A second determination is made as to how the set of anode currents designated for the first electroplating cycle should be varied. See the third and sixth method steps of claim 1 on page 10 of ***Wilson***.

Wilson does not teach or suggest selectively revising a chemical concentration parameter of a deposition recipe to produce a desired thickness based on the measured thickness. ***Wilson*** refines electrical parameters to produce a specified target plating material thickness of a workpiece. Accordingly, ***Wilson*** does not teach or make obvious measuring a plating material thickness. In contrast to ***Wilson***, the claimed invention in claims 1 and 6 require that the plating material thicknesses be measured to produce a desired thickness. Further, as discussed below, ***Uzoh*** does not make up for the deficit of ***Wilson***.

The Examiner concedes that ***Wilson*** fails to teach or suggest the limitation in independent claim 1 of "revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance." Final

Office Action at page 2. The Examiner relies on ***Uzoh*** to make obvious this limitation. However, ***Uzoh*** also fails to teach or make obvious either expressly or under principles of inherency, revising the chemical concentration parameter of an electroplating bath of the deposition recipe itself across the entire conductive layer based on the measured thickness of the conductive layer. Therefore, neither ***Wilson*** nor ***Uzoh*** provide any suggestion to modify or combine the prior art as suggested by the Examiner so as to arrive at Applicant's claimed invention.

In rejecting claims 1 and 6, the Examiner asserts that ***Wilson*** inherently teaches depositing a conductive layer above a second semiconductor wafer based upon the revised deposition recipe. The Examiner further suggests that it is inherent that in every electroplating bath process the plating measured thickness of the conductive layer is proportional to the chemical concentration. That is, the Examiner reasons that the combination of ***Wilson*** and ***Uzoh*** teaches the claimed invention because both the ***Wilson*** and ***Uzoh*** references are related to a method of controlling a conductive layer deposition process that uses electroplating bath. Applicants respectfully disagree with this reasoning. However, the Examiner fails to provide evidence or arguments as to why ***Wilson*** inherently teaches depositing a conductive layer above a second semiconductor wafer based upon the revised deposition recipe. The Examiner merely asserts that depositing a conductive layer above a second semiconductor wafer according to the revised deposition recipe based upon the measured thickness of the conductive layer is inherent but does not support this assertion with evidence of reasoning.

In the Final Office Action, the Examiner seems to imply that ***Uzoh*** produces a desired physical aspect in a microelectronic workpiece on a semiconductor wafer substrate by

controlling an electrical aspect for modifying a chemical aspect of a material deposition process in an automatic process control. For example, by modifying the localized concentration of ions in the electrolytic bath partially and across only certain parts of a target film in a microelectronic workpiece, ***Uzoh*** produces a plating material thickness. However, ***Uzoh*** does not measure a physical aspect, such as the measured plating material thickness. Therefore, Appellants respectfully disagree with Examiner's reasoning since this assertion is not supported at all by the disclosure of ***Uzoh***.

Uzoh discloses enhancing the uniformity of electrodeposition or electroetching to uniformly deposit or etch a thin metal layer or an alloy layer on a semiconductor wafer substrate. By modifying the localized concentration of ions in the electrolytic bath in contact with different parts of a target film, more uniform electroetched or electroplated films in electroetching and electroplating processes are produced. Thus, the uniformity is enhanced by modifying the current flow or by shaping the potential field between anode and cathode (the workpiece or wafer) and the localized current flow rate, as it approaches the electroetching or electroplating target. See Col. 2 ll. 58-67. However, ***Uzoh*** does not teach or make obvious the concept of selectively revising a chemical concentration parameter of the electroplating bath of the deposition recipe across the entire conductive layer based on the measured thickness of the conductive layer. ***Uzoh*** discloses enhancing the uniformity of electrodeposition or electroetching, which is not related to revising of a chemical concentration parameter to produce a desired plating material thickness based on the measured thickness of the plating material layer. ***Wilson*** does not teach or make obvious this subject matter. Therefore, ***Uzoh*** fails to compensate for the deficit of ***Wilson***.

Uzoh does not disclose or make obvious "selectively revising a chemical concentration parameter of the deposition recipe itself across the entire conductive layer to produce a desired physical aspect based on a measurement of the physical aspect of a structure deposited on a semiconductor wafer." Since neither ***Uzoh*** nor ***Wilson*** disclose or make obvious the subject matter of revising a chemical concentration parameter to produce a desired plating material thickness based on the measured thickness of the plating material layer, it is respectfully submitted that the combination of ***Wilson*** and ***Uzoh*** fails to present a *prima facie* case of obviousness with respect to claimed invention set forth in independent claims 1 and 6, respectfully.

Additionally, those skilled in the art would not combine ***Wilson*** and ***Uzoh*** to make obvious all of the elements of the claimed invention. However, the Examiner alleges that those skilled in the art would combine teachings of ***Wilson*** and ***Uzoh*** to make obvious all the elements of claim 1. Appellants respectfully disagree. The purpose of ***Wilson's*** method and apparatus is to refine electrical parameters to produce a specified target plating material thicknesses rather than use the measured plating material thicknesses of a workpiece. The purpose of ***Uzoh's*** method is to enhance the uniformity of electrodeposition or electroetching but not through a deposition process that controls a chemical aspect of the deposition recipe itself across the entire conductive layer, let alone based on the measured thickness of the conductive layer. These are vastly different subject matter that does not disclose sufficient motivation to combine with each other. ***Uzoh*** fails to provide any suggestion or motivation to modify the ***Wilson*** method in any way to produce the Applicants' claimed invention. Appellants, thus, respectfully assert that the prior art fails to provide any suggestion or motivation to modify ***Wilson*** or to combine ***Wilson*** and ***Uzoh*** to make obvious the claims of the present invention.

Using the Examiner's reasoning, if one of ordinary skill in the art at the time of the invention were to combine the teachings of ***Wilson*** and ***Uzoh***, the result would not be a deposition process that selectively controls a chemical aspect of the deposition recipe itself across the entire conductive layer based on a measurement of a physical aspect of a structure deposited on a semiconductor wafer. Therefore, the combination of ***Wilson*** and ***Uzoh*** could not disclose or make obvious all of the elements of claim 1. Furthermore, neither ***Wilson*** nor ***Uzoh*** reference provides any suggestion or motivation to modify the reference or to combine reference teachings to arrive at Applicants' claimed invention. Thus those skilled in the art would not combine ***Wilson*** and ***Uzoh*** to make obvious claim 1 of the present invention.

The combination ***Wilson*** and ***Uzoh*** simply results in an automatic process control that controls an electrical aspect for modifying a chemical aspect of a material deposition process partially (e. g., modifying the localized concentration of ions in the electrolytic bath). The combination refers to performing this task across only certain parts of a target film in a microelectronic workpiece to produce a desired physical aspect (*e.g.*, a plating material thickness) on a semiconductor wafer substrate rather than using a measurement of a physical aspect, such as the measured plating material thickness. Thus, as set forth herein, the combination of the ***Wilson*** and ***Uzoh*** does not disclose or make obvious all claim elements in claim 1.

Additionally, ***Wilson*** teaches away from using ***Uzoh*** to make obvious all claim elements in claim 1. Rather than using the measured plating material thicknesses of a conductive layer on a workpiece to produce a desired thickness of the conductive layer based on a chemical adjustment of the deposition recipe, ***Wilson's*** refines electrical parameters to produce a specified

target plating material thicknesses. In contrast, ***Uzoh*** enhances the uniformity of electrodeposition or electroetching through a deposition process that does not control a chemical aspect of the deposition recipe itself across the entire conductive layer. Therefore, ***Wilson*** and ***Uzoh*** teach away from claim 1. In contrast to both ***Wilson*** and ***Uzoh,*** claim 1 calls for revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance. One skilled in the art would be directed away from claim 1 because combining subject matter of ***Wilson*** and subject matter of ***Uzoh*** would lead one away from selectively using the measured plating material thicknesses of a conductive layer on a workpiece to produce a desired thickness of the conductive layer based on a chemical adjustment of the deposition recipe. There can be no motivation or suggestion to combine references as a matter of law where one of the references teaches away from the claimed invention. *In re Fine*, 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *Gordon*, 1127. As discussed above, ***Wilson*** and ***Uzoh*** teach away from the claimed invention. Therefore, there is no motivation to combine the teachings of ***Wilson*** and ***Uzoh***. Accordingly, one skilled in the art would not combine the teachings of ***Wilson*** and ***Uzoh***. Thus, the Examiner's obviousness rejection of claims 1 and 6 based upon the combination of ***Wilson*** and ***Uzoh*** was improper. Moreover, there is simply no suggestion in ***Wilson*** and ***Uzoh*** to modify these teachings so as to arrive at the invention defined by independent claims 1 and 6, respectfully. In view of the foregoing, it is respectfully submitted that the Examiner erred in rejecting independent claims 1 and 6 and all claims depending therefrom. Applicant respectfully requests that the Board reverse the Examiner's rejection of claims 1, 2 and 6-12.

For at least the aforementioned reasons, Appellants respectfully submit that the remarks provided above concerning independent claim 1 apply equally to independent claim 6 since ***Wilson*** and ***Uzoh***, either alone or in combination, fail to teach or suggest all the limitations of rejected independent claim 6 as a whole and thus this claim is not rendered obvious in a *prima facie* manner over ***Wilson*** in view of ***Uzoh***. Thus, independent claim 6 is also allowable for at least the reasons cited above. Additionally, dependent claims 2 and 7-12, which depend from independent claims 1 and 6, respectively, are also allowable for at least the reasons cited above. Accordingly, the Examiner's rejections of 1, 2 and 6-12, which stand or fall together, should be reversed.

Group II Claims (Claims 4 and 15) Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Wilson* in view of *Uzoh*

As described above, ***Wilson***, ***Uzoh***, nor their combination, disclose or make obvious revising the chemical concentration parameter of an electroplating bath of the deposition recipe itself across the entire conductive layer based on the measured thickness of the conductive layer, as called for by Group I claims by virtue of their direct or indirect dependencies to claims 1 and 6. Additionally, ***Wilson***, ***Uzoh***, nor their combination, disclose or make obvious depositing a conductive layer above a second semiconductor wafer based upon the revised deposition recipe, as called for by Group II claims by virtue of their direct or indirect dependencies. Therefore, these additional features called for by Group II claims are not disclosed or made obvious by ***Wilson***, ***Uzoh***, nor their combination.

Hence, Group II claims (claims 4, and 15) are not disclosed or made obvious by ***Wilson***, ***Uzoh***, nor their combination, and therefore, are also allowable. Accordingly, Appellants

respectfully assert that the Examiner erred in rejecting claims 4, and 15 under 35 U.S.C. § 103(a) because the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness based upon ***Wilson***, ***Uzoh***, or their combination. Therefore, claims 4 and 15 are allowable and the Board should reverse the Examiner's rejection of claims 4 and 15.

Group III Claims (Claims 5 and 13) Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Wilson* in view of *Uzoh*

As described above, ***Wilson***, ***Uzoh***, nor their combination, disclose or make obvious revising the chemical concentration parameter of an electroplating bath of the deposition recipe itself across the entire conductive layer based on the measured thickness of the conductive layer as called for by Group III claims by virtue of their direct or indirect dependencies to claims 1 and 6. Additionally, ***Wilson***, ***Uzoh***, nor their combination, disclose or make obvious revising the deposition recipe according to at least one predetermined model, as respectively called for by claims 5 and 13 (Group III claims). Therefore, these additional features called for by Group III claims are not disclosed or made obvious by ***Wilson***, ***Uzoh***, nor their combination.

Hence, Group III claims (claims 5 and 13) are not disclosed or made obvious by ***Wilson***, ***Uzoh***, nor their combination, and therefore, are also allowable. Accordingly, Appellants respectfully assert that the Examiner erred in rejecting claims 5 and 13 under 35 U.S.C. § 103(a) because the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness based upon ***Wilson***, ***Uzoh***, or their combination. Therefore, claims 5 and 13 are in condition for allowance and the Board should reverse the Examiner's rejection thereof.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – Claims 1, 2, 4-13, and 15 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

There is no separate Evidence Appendix for this appeal.

X. RELATED PROCEEDINGS APPENDIX

There is no Related Proceedings Appendix for this appeal.

XI. CONCLUSION

In view of the foregoing, Applicants respectfully submit that the Examiner's assertion that the inventions defined in the pending claims are obvious in view of ***Wilson*** and ***Uzoh***, or any other art of record, necessarily involved an improper use of hindsight using Applicant's disclosure as a roadmap. A recent Federal Circuit case makes it crystal clear that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. Accordingly, it is respectfully submitted that the Examiner erred in not allowing claims 1, 2, 4-13, and 15 over the prior art of record. Applicant respectfully requests the Board reverse the Examiner's rejections. The undersigned attorney may be contacted at (713) 934-4089 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,
WILLIAMS, MORGAN & AMERSON
CUSTOMER NO. 23720

Date: June 6, 2005

Jaison C. John
Reg. No. 50,737
Attorney for Applicants

WILLIAMS, MORGAN & AMERSON
CUSTOMER NUMBER: 23720
10333 Richmond Dr., Suite 1100
Houston, Texas 77042
(713) 934-4069 ph
(713) 934-7011 fx

CLAIMS APPENDIX

1. A method of controlling a conductive layer deposition process, comprising:

depositing a conductive layer above a first semiconductor wafer based upon a deposition recipe;

measuring a thickness of the conductive layer deposited on the semiconductor wafer;

determining whether the measured thickness of the conductive layer is within a predetermined tolerance; and

revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance.

2. A method, according to claim 1, wherein:

depositing the conductive layer above the first semiconductor wafer further comprises depositing a copper layer above the first semiconductor wafer;

measuring the thickness of the conductive layer further comprises measuring the thickness of the copper layer;

determining whether the measured thickness of the conductive layer is within the predetermined tolerance further comprises determining whether the measured thickness of the copper layer is within the predetermined tolerance; and

revising the deposition recipe further comprises revising the deposition recipe if the measured thickness of the copper layer is not within the predetermined tolerance.

3. (canceled)

4. A method, according to claim 1, further comprising depositing a conductive layer above a second semiconductor wafer based upon the revised deposition recipe.

5. A method, according to claim 1, wherein revising the deposition recipe further comprises revising the deposition recipe according to at least one predetermined model.

6. A method of controlling a conductive layer deposition process, comprising:

depositing a conductive layer above a first semiconductor wafer based upon a deposition recipe;

measuring a thickness of the conductive layer at a plurality of locations;

calculating a value representing the measured thickness measured at the plurality of locations;

determining whether the calculated value is within a predetermined tolerance; and

revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe based upon at least the calculated value if the calculated value is not within the predetermined tolerance.

7. A method, according to claim 6, wherein:

depositing the conductive layer above the first semiconductor wafer further comprises depositing a copper layer above the first semiconductor wafer; and

measuring the thickness of the conductive layer further comprises measuring the thickness of the copper layer at the plurality of locations.

8. A method, according to claim 6, wherein measuring the thickness of the conductive layer further comprises measuring the thickness of the conductive layer in a predetermined pattern of locations.

9. A method, according to claim 6, wherein calculating the value further comprises calculating an average of the plurality of thickness measurements.

10. A method, according to claim 6, wherein calculating the value further comprises calculating the value selected from the group consisting of an arithmetic mean of the plurality of thickness measurements, a median of the plurality of thickness measurements, a mode of the plurality of thickness measurements, a geometric mean of the plurality of thickness measurements, a harmonic mean of the plurality of thickness measurements, and a quadratic mean of the plurality of thickness measurements.

11. A method according to claim 6, wherein determining whether the thickness of the conductive layer is within the predetermined tolerance further comprises calculating a measure of a degree of dispersion of the plurality of thickness measurements about the calculated value and comparing the measure of the degree of dispersion to a predetermined statistical distribution.

12. A method, according to claim 6, wherein determining whether the thickness of the conductive layer is within the predetermined tolerance further comprises calculating a measure of a degree of dispersion of the plurality of thickness measurements about the calculated value representing the measured thicknesses and comparing the measure of the degree of dispersion to a distribution selected from the group consisting of a normal distribution, a binomial distribution, a Poisson distribution, and a multinomial distribution.

13. A method, according to claim 6, wherein revising the deposition recipe further comprises revising the deposition recipe according to at least one predetermined model.

14. (canceled)

15. A method, according to claim 6, further comprising depositing a conductive layer above a second semiconductor wafer based upon the revised deposition recipe.